

Features

- Uses PingWei advanced PerfectMOS technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- Excellent Low Ciss
- Qualified according to JEDEC criteria

Benefits

- High robustness and reliability
- Increases maximum current capability
- Low power loss, high power density
- Easy paralleling

Applications

- Synchronous Rectification for AC/DC Quick Charger
- Battery management
- UPS (Uninterruptible Power Supplies)

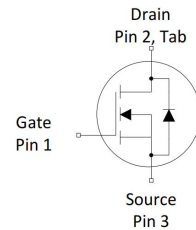
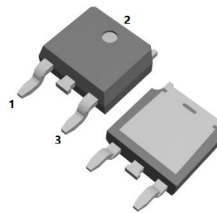


100% DVDS Tested
100% Avalanche Tested

Product Summary

V_{DS}	100V
$R_{DS(on)@10V}$ typ	5mΩ
I_D	80A

TO-252-2L



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
PW060N10GS	060N10GS	TO-252-2L	Tape&Reel	13 inches	16mm	2500pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Continuous drain current	I_D	100	A
$T_C = 25^\circ\text{C}$ (Silicon limit)		80	
$T_C = 25^\circ\text{C}$ (Package limit)		63	
$T_C = 100^\circ\text{C}$ (Silicon limit)		10	
$T_a = 25^\circ\text{C}$			
Pulsed drain current ($T_C = 25^\circ\text{C}$, $t_p = 100\mu\text{s}$)	$I_{D\ pulse}$	320	A
Avalanche energy, single pulse ($L=0.5\text{mH}$, $V_{ds}=50\text{V}$)	E_{AS}	90	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation	P_{tot}	104	W
$T_C = 25^\circ\text{C}$		1.1	
$T_a = 25^\circ\text{C}$			
Operating junction and storage temperature	T_j, T_{stg}	-55...+150	$^\circ\text{C}$
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	T_{sold}	260	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – case.	RthJC	-	-	1.2	°C/W	-
Thermal resistance, junction - ambient(min. footprint)	RthJA	-	-	114	°C/W	-

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV_{DSS}	100	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{GS(th)}$	2.0	-	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	0.02	1	μA	$V_{DS}=100V, V_{GS}=0V$ $T_j=25^\circ C$ $T_j=150^\circ C$
Gate-source leakage current	I_{GSS}	-	± 10	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	5.0	6.0	mΩ	$V_{GS}=10V, I_D=50A$
Transconductance	g_{fs}	-	55	-	S	$V_{DS}=5V, I_D=50A$

Dynamic Characteristic

Input Capacitance	C_{iss}	-	2509	-	pF	$V_{GS}=0V, V_{DS}=50V,$ $f=1MHz$
Output Capacitance	C_{oss}	-	543	-		
Reverse Transfer Capacitance	C_{rss}	-	26	-		
Gate Total Charge	Q_G	-	41	-	nC	$V_{DS}=50V, I_D=50A,$ $V_{GS}=10V$
Gate-Source charge	Q_{gs}	-	15	-		
Gate-Drain charge	Q_{gd}	-	10	-		
Turn-on delay time	$t_{d(on)}$	-	16.8	-	ns	$V_{GS}=10V, V_{DD}=50V,$ $R_{G_ext}=1.6\Omega, I_D=50A$
Rise time	t_r	-	56.4	-		
Turn-off delay time	$t_{d(off)}$	-	32	-		
Fall time	t_f	-	11	-		
Gate resistance	R_G	-	1.6	-	Ω	$V_{GS}=0V, V_{DS}=0V,$ $f=1MHz$



Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	-	1.2	V	$V_{GS}=0V, I_{SD}=50A$
Body Diode Continuous Forward Current	I_S	-	-	80	A	$TC = 25^{\circ}C$
Body Diode Pulsed Current	I_S pulse	-	-	320	A	$TC = 25^{\circ}C$
Body Diode Reverse Recovery Time	t_{rr}	-	48	-	ns	$I_F=50A, dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	-	54	-	nC	



Typical Performance Characteristics

Fig 1: Output Characteristics

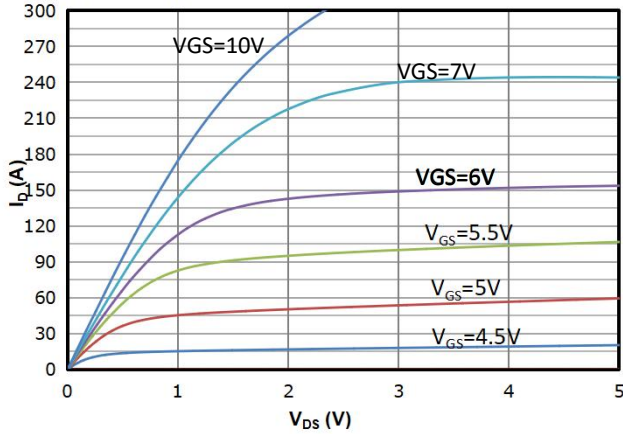


Fig 2: Transfer Characteristics

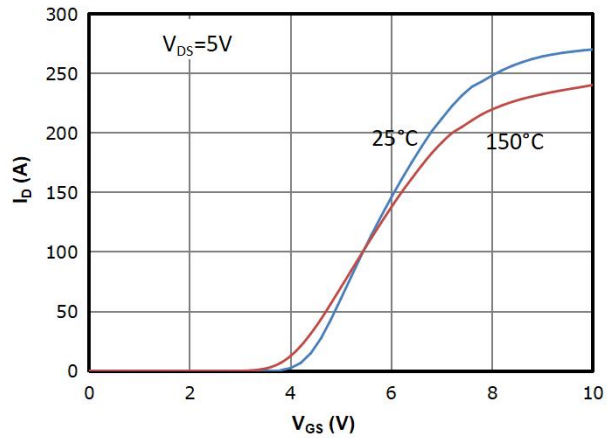


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

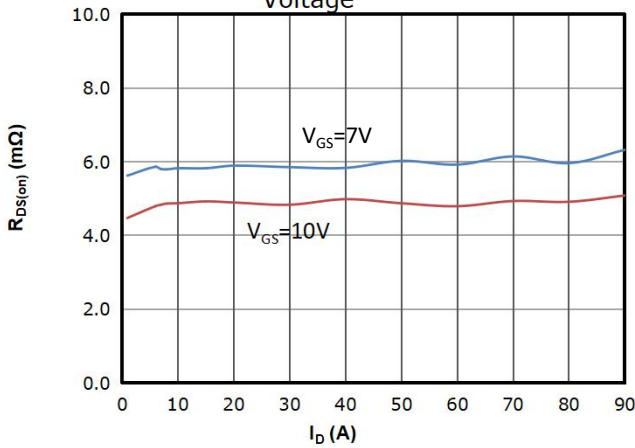


Fig 4: $R_{DS(on)}$ vs Gate Voltage

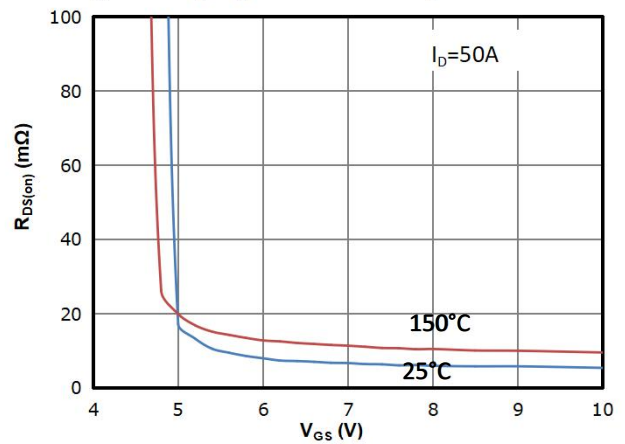


Fig 5: $R_{DS(on)}$ vs. Temperature

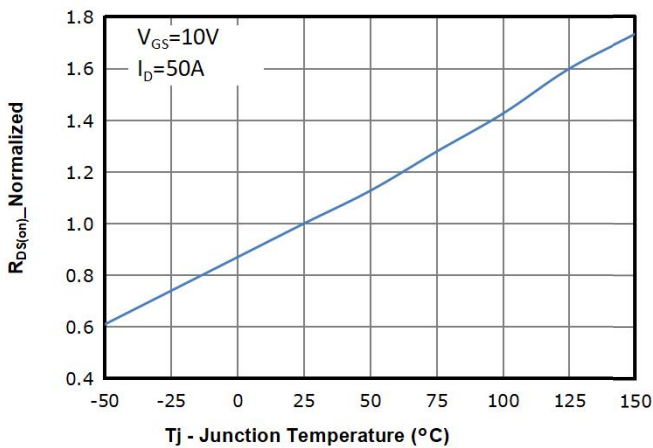


Fig 6: $V_{GS(th)}$ vs. Temperature

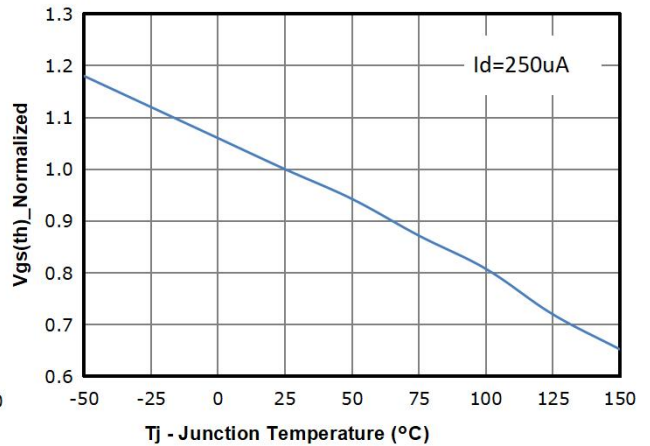




Fig 7: BVdss vs. Temperature

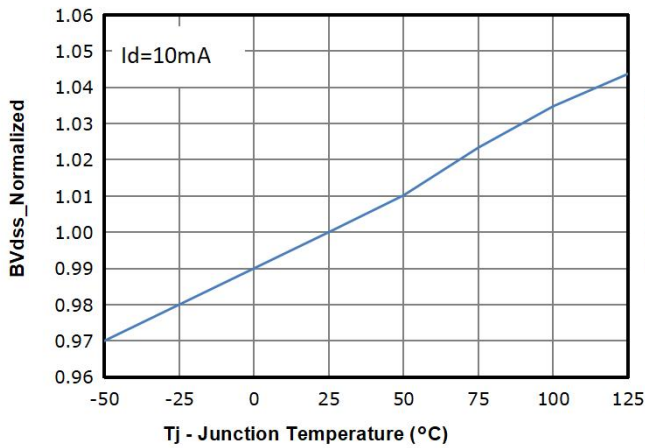


Fig 8: Capacitance Characteristics

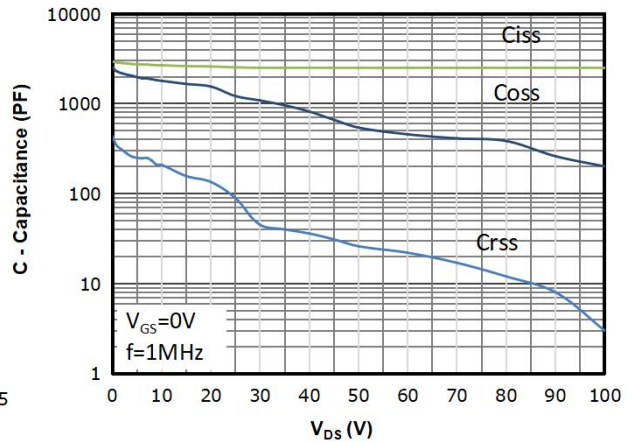


Fig 9: Gate Charge Characteristics

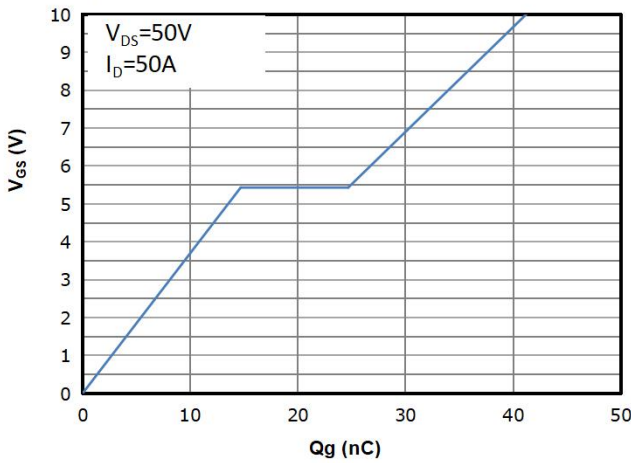


Fig 10: Body-diode Forward Characteristics

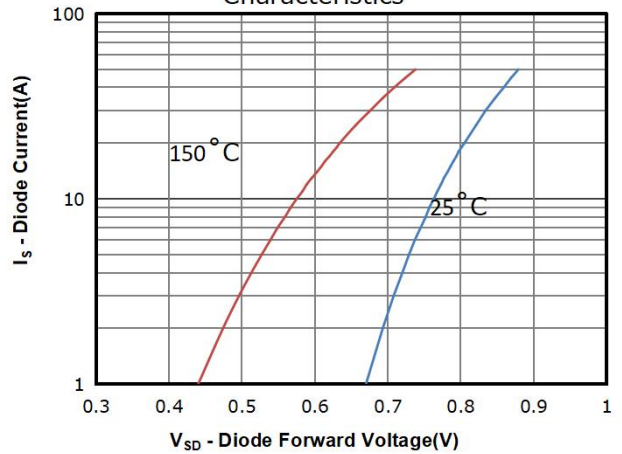


Fig 11: Power Dissipation

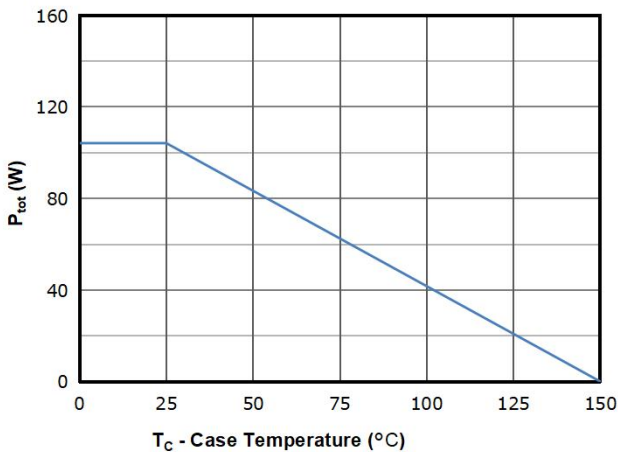


Fig 12: Drain Current Derating

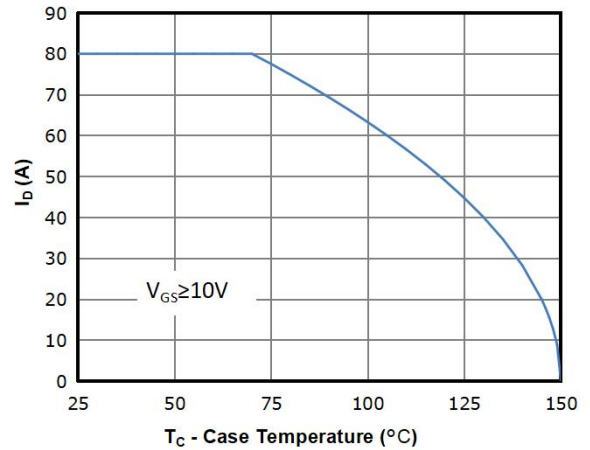




Fig 13: Safe Operating Area

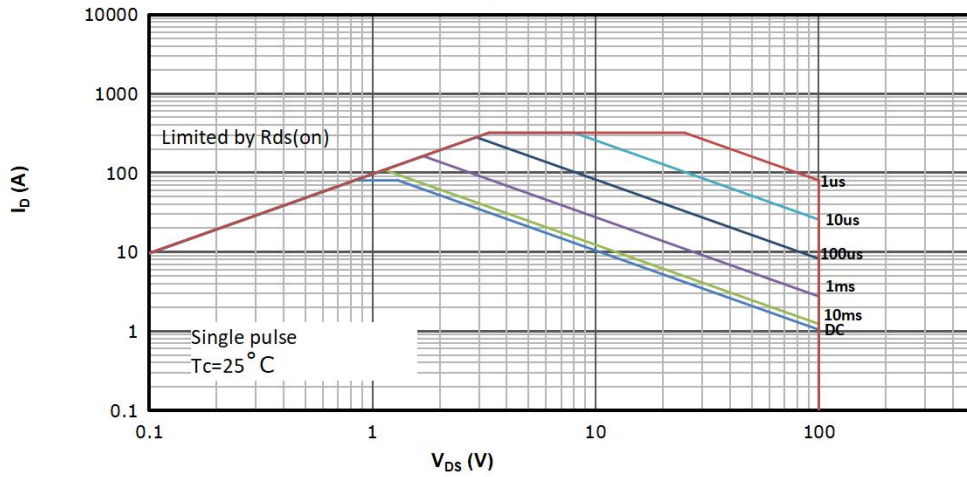
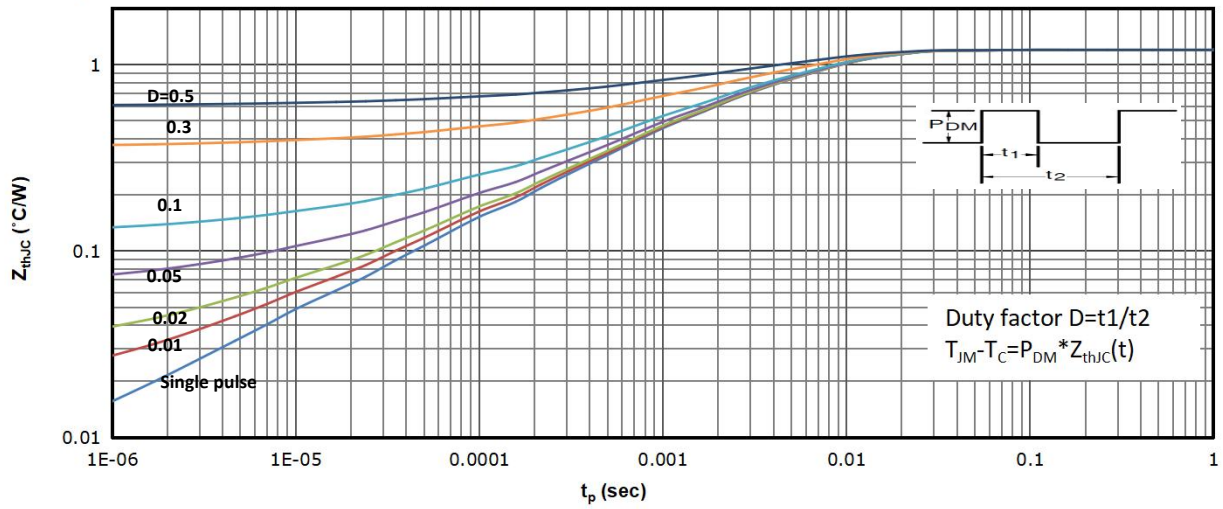
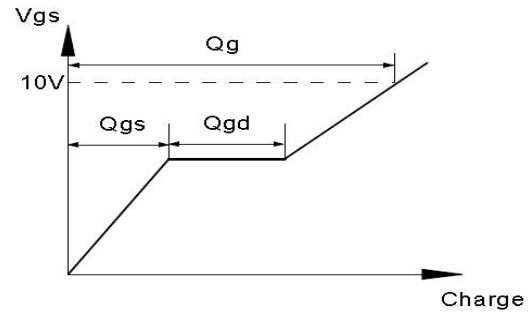
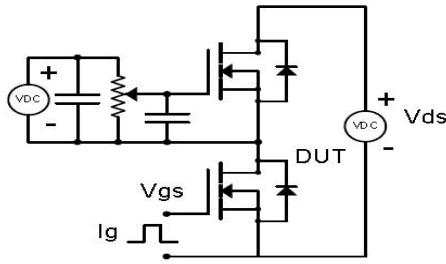


Fig 14: Max. Transient Thermal Impedance

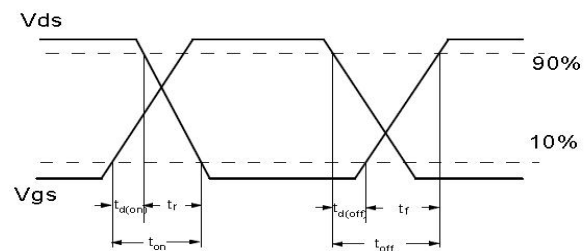
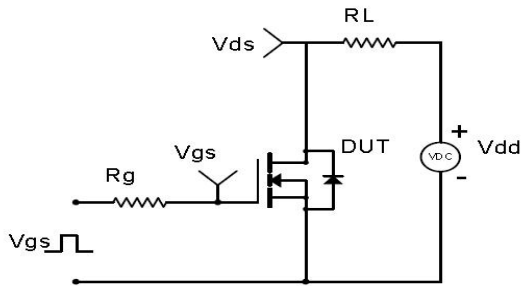


Test Circuit & Waveform

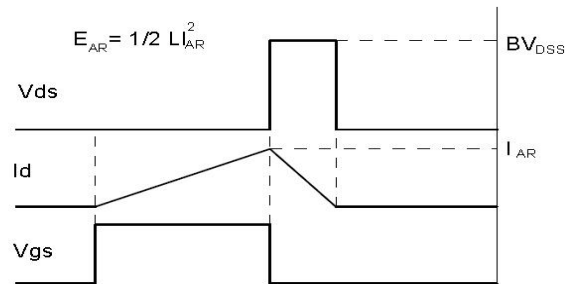
Gate Charge Test Circuit & Waveform



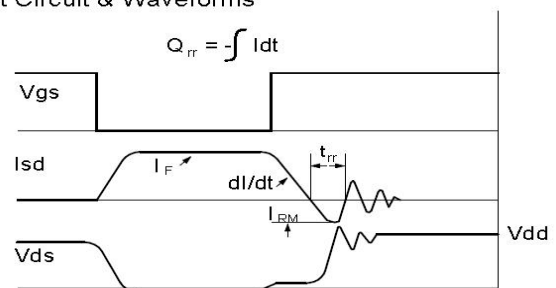
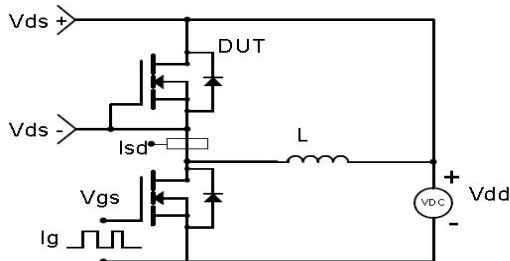
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

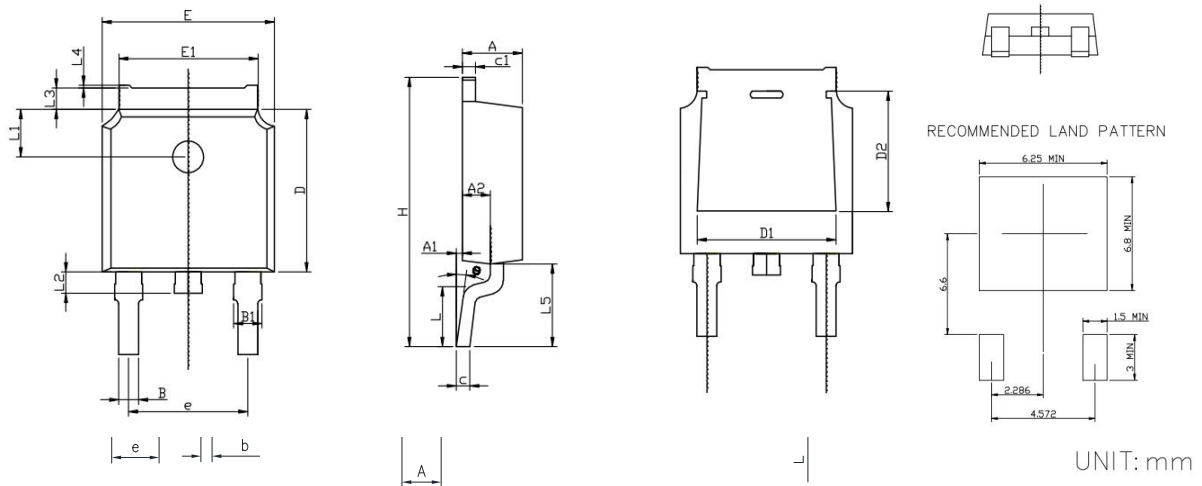


Diode Recovery Test Circuit & Waveforms





Package Outline: TO-252-2L



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.15	2.45	0.085	0.096
A1	0.05	0.20	0.002	0.008
A2	0.91	1.22	0.036	0.048
B	0.66	0.86	0.026	0.034
B1	0.93	1.23	0.037	0.048
C	0.40	0.60	0.016	0.024
C1	0.40	0.60	0.016	0.024
D	5.95	6.25	0.234	0.246
D1	4.80		0.189	
D2	3.80		0.150	
E	6.45	6.75	0.254	0.266
E1	5.12	5.52	0.202	0.217
L	1.65		0.065	
L1	1.58	1.98	0.062	0.078
L2	0.60	1.00	0.024	0.039
L3	0.70	1.00	0.028	0.039
L4	0.00	0.20	0.000	0.008
L5	2.80	3.40	0.110	0.134
H	9.80	10.40	0.386	0.409
θ	0.00	8.00	0.000	0.315
e	4.57		0.180	



Revision History

Revision	Date	Major changes
1.0	2023/7/17	Release of Formal Version.

Disclaimer

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

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